Strategy of selecting power reduction technique for energy-efficient semiconductor designs

P.V. Parnevich
dept. of Computer Engineering
Vladimir State University
Vladimir, Russia
e-mail: PVParnevich@gmail.com

S.G. Mosin
dept. of Computer Engineering
Vladimir State University
Vladimir, Russia
e-mail: smosin@vpti.vladimir.ru

***Abstract* – There are a lot of techniques, which oriented on power consumption reducing. Unfortunately, there is no such method that is able to meet all the system requirements for energy minimization. This paper presents a strategy of power reduction technique selecting that can be used to make effective decisions in developing energy-efficient semiconductor designs. Techniques operating at synchronous and asynchronous schemes are described, including dynamic voltage and frequency scaling, clock gating, state-retention power gating and others.**

Keywords-energy-efficient technique; clock gating; power gating; dual voltage scheme; GALS

1. Introduction

The design of an electronic system is almost always constrained by power and energy considerations – whether it is battery life for a mobile device, thermal power dissipation in a high-performance processor or ultra-low power consumption for a wireless sensing application. In addition, recent economic forces and increased environmental awareness have changed the landscape for new product design. Now energy efficiency is often the lead discussion as companies formulate new product strategies. However, even though energy budgets are playing a larger role in determining the finished designs, manufacturers realize that the market will not allow them to compromise on performance.

There are some techniques, like GALS (globally asynchronous, locally synchronous) systems [1], DVFS (dynamic voltage and frequency scaling) based techniques [2], clock gating [3], state-retention power gating (SRPG) techniques [4], which oriented on power consumption reducing.

Unfortunately, there is no single power reduction technique that is able to meet all the system requirements for energy minimization. The trick is to effectively combine different techniques to intelligently develop energy-efficient semiconductor designs.

This paper presents a strategy of power reduction technique selecting that can be used to make effective decisions in developing energy-efficient semiconductor designs.

2. Synchronization strategy selecting

The scientific community is showing great interest in GALS solutions and architectures nowadays due to their high performance. However, sometimes it's profitably to use fully synchronous schemes, because synchronous digital design is well understood and the design methodology and flow are established. Thereby it's necessary to care about guaranteeing energy efficiency in both cases.

2.1. GALS systems

A GALS system consists of complex digital blocks operating synchronously. Those blocks are usually developed using standard synchronous CAD tools and design flow. However, the operation of the blocks is not mutually synchronized – hence the term locally synchronous. These locally synchronous blocks communicate with one another asynchronously by using handshaking protocol.

Since each block is in its own frequency domain, it becomes possible to reduce the power dissipation and increase energy efficiency in many ways:

- GALS clocking design allows to utilize simple local ring oscillator for each core, and hence eliminates the need of complex and power hungry global clock trees [5].
- Unused cores can be effectively disconnected by power gating, and thus reducing leakage.
- When workloads distributed for cores are not identical, we can allocate different clock frequencies and supply voltages for these cores either statically or dynamically. This allows the total system to consume a lower power than if all active cores had been operating at a single frequency and supply voltage [6].

However, there are several reasons why standard design practice has not adopted GALS techniques. Ring oscillators are impractical for industrial use. They need careful calibration because they are very sensitive to process, voltage, and temperature variations. Moreover, embedded ring oscillators consume additional power through continuous switching of the chained inverters.

Another significant drawback is that functional test of asynchronous circuits is very difficult because most ATE (Automatic Test Equipment) is cycle based and cannot provide event-based handshake signals. For GALS circuits, the process of arbitration and stretching leads to nondeterministic timing behavior. Therefore, the test result can differ from chip to chip and from test run to test run.

2.2. Synchronous schemes

Like in GALS systems there are many ways to increase energy efficiency in synchronous schemes.

- DVFS allows on-the-fly frequency adjustment according to existing system performance requirements. By lowering the frequency, it is possible to lower the operating voltage (on-the-fly as well), dramatically reducing the power consumption. A drawback of the proposed approach is a reduction in reliability, resulting from the lower link voltage.
- Clock gating is an effective strategy that is widely used to help reduce power consumption while maintaining the same levels of performance and functionality. A circuit uses more power when it's being clocked than when the clock is gated or turned off. Clocks can consume as much as 40 percent of active power. Shutting off the clocks and stopping the data toggling in unused portions of the semiconductor brings sizable energy saving. In this case the organization of clock management becomes a crucial task.
- SRPG is a technique that allows the voltage supply to be reduced to zero for the majority of a block's logic gates while maintaining the supply for the state elements of that block. SRPG can thereby greatly reduce power consumption when the application is in stop mode, yet it still accommodates fast wake up times. Reducing the supply to zero in stop mode allows both dynamic and static power to be removed. Retaining the supply on the state elements allows processing to continue quickly when exiting stop mode.The quality of complex power network is critical to the success of a power-gating design.

3. Energy-efficient technique appliance

The effective combination of energy-efficient techniques was presented in [7]. The main idea of the proposed design is to implement a complete Dynamic Voltage and Frequency Scaling architecture within a complex GALS NOC.

Each units of the dedicated SoC are arranged around a fully asynchronous Network-on-Chip. As shown Figure 1, the NoC units are fully synchronous islands. Synchronization between the communication router and the units is done thanks to a pausable clock mechanism called SAS (containing Synchronous-to-Asynchronous and Asynchronous-to-Synchronous interfaces). A programmable Local Clock Generator (LCG), using a delay line, is implemented within each unit to generate a variable frequency in a predefined applicative range. The power unit manages the local unit voltage, sharing a power switch between a V_{DD} hopping technique and an ultra-cut-off block. The Power Unit uses two external voltages : V_{HIGH} and V_{LOW} to be automatically switched during DVS phases. The Network Interface (NI) is in charge of communications with respect to NoC protocol and is also in charge of local voltage and frequency control for DVFS using a Low Power Manager.

The power management strategy is programmed by the main CPU, through NoC unit attached Network Interface's Low Power Managers, according to required performance and power constraints. DVFS can be executed during IP computation and communication according to their own activity. The only global signals are regarding units' reset and off control. The main CPU is required to directly disable/enable the units for power off mode and the corresponding reset phase.

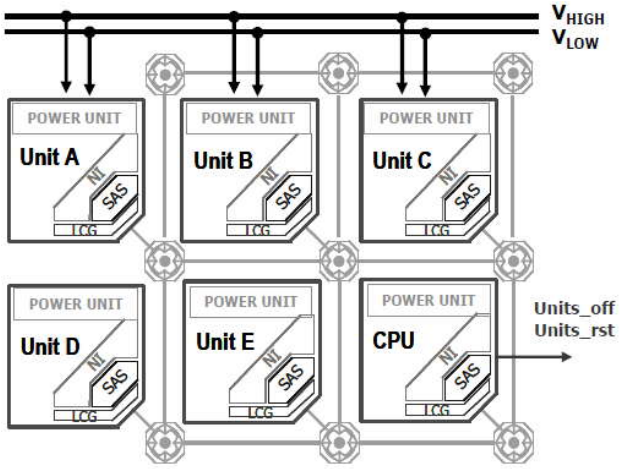

Figure 1. DVFS NOC architecture.

The power efficiency of the proposed system has been evaluated close to 95%.

4. Conclusion

All the described methods are oriented on energy minimization. The trick is to learn how to use and combine them effectively to reach more energy savings. This paper presented a strategy of power reduction technique selecting that can be used to create low energy designs.

References

[1] Miloš Krstić, Eckhard Grass, Frank K. Gürkaynak, Pascal Vivet, "Globally Asynchronous, Locally Synchronous Circuits: Overview and Outlook", IEEE Design & Test, v.24 n.5, pp.430-441, September 2007, doi:10.1109/MDT.2007.164.

[2] Wen-Yew Liang, Shih-Chang Chen, Yang-Lang Chang, and Jyh-Perng Fang, "Memory-aware dynamic voltage and frequency prediction for portable devices", Proc. 14th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'08), August 2008, pp. 229-236, doi: 10.1109/RTCSA.2008.19.

[3] Jithendra Srinivas, Madhusudan Rao, S. Jairam, H. Udayakumar, Jagdish Rao, "Clock gating effectiveness metrics: Applications to power optimization", Proc. 10th International Symposium on Quality of Electronic Design, pp. 482-487, doi:10.1109/ISQED.2009.4810342.

[4] Kanak Agarwal, Kevin Nowka, Harmander Deogun, Dennis Sylvester, "Power Gating with Multiple Sleep Modes", Proc. 7th International Symposium on Quality Electronic Design, pp.633-637, March 27-29, 2006 , doi:10.1109/ISQED.2006.102.

[5] V. Tiwari, D. Singh, et al., "Reducing power in high-performance microprocessors", Proc. 35th annual Design Automation Conference, pp. 732 – 737, June 1998.

[6] Sebastian Herbert, Diana Marculescu, "Analysis of dynamic voltage/frequency scaling in chip-multiprocessors", Proc. 2007 international symposium on Low power electronics and design, pp. 38 – 43, August 27-29, 2007.

[7] E. Beign´e, F. Clermidy, S. Miermont, and P. Vivet, "Dynamic voltage and frequency scaling architecture for units integration within a GALS NoC," in Network on Chip, Proc. International Symposium, pp. 129–138, 2008, doi:10.1109/NOCS.2008.26.